

E10 EM series

Series/Type: Ordering code: B78307A\*A003

Date: 2020-05-06

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## E10 EM series B78307A\*A003

#### Construction

- Ferrite core MnZn
- SMD gullwing pins
- Triple insulated wire
- Non-conductive pick-and-place cap on top

#### **Features**

- Height: 11.35 mm max
- Design in compliance with IEC 61558-1; 2-16<sup>1</sup>, 61800-5-1<sup>1</sup>, IEC 60664-1<sup>1,2</sup>
- UL1446 class 155(F) electrical insulation system
- Wide temperature range up to +150 °C
- Qualified to AEC-Q200
- RoHS compatible

## **Applications**

- Isolated DC/DC converters (bridge and flyback topology)
- Gate driver circuits (e.g.1DE020I12FA, for 650 V IGBTs)
- Digital isolator ICs (e.g.Si88xx)

## Insulation characteristics

- N1 / N2 creepage ≥ 6 mm, clearance ≥ 5.5 mm (cumulative, core is conductive, free floated between N1 and N2)
- [N1,N2] / [core] creepage ≥ 3 mm, clearance ≥ 2.75 mm
- Top surface / core creepage and clearance ≥ 2 mm
- Plastic materials UL94-V0, CTI ≥175
- Insulated wire UL60950-1, Annex U
- Reinforced insulation<sup>1</sup> N1 / N2 working voltage 300 V
- Basic insulation<sup>2</sup> N1 / N2 working voltage 500 V

### Marking

Product brand, middle block of ordering code, date code, pin 1 marker, production place identification code

## **Delivery mode**

- Blister tape 380 mm diameter
- Packing unit 280 pcs per reel

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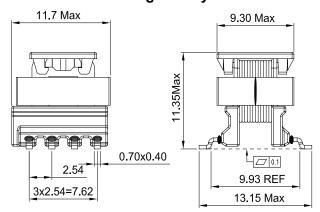
<sup>&</sup>lt;sup>1</sup> Overvoltage category OVC II, pollution degree P2, CTI ≥ 175, altitude ≤ 2 km

<sup>&</sup>lt;sup>2</sup> Overvoltage category OVC II, pollution degree P2, CTI ≥ 175, altitude ≤ 5 km

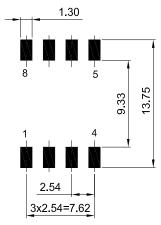


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# Dimensional drawing and layout recommendation

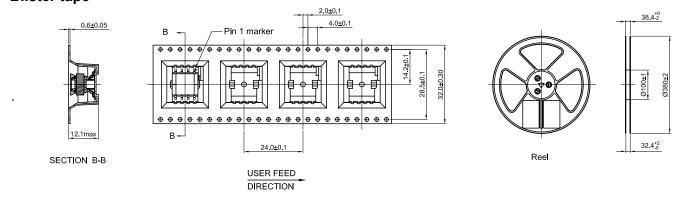


Recommended PCB layout (Top View)



Dimensions in mm

# Blister tape



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# Technical data and measuring conditions

Specified @ +25 °C if not mentioned otherwise, all values without tolerance are typical values

•
100 500 kHz (typ.)
3000 V AC (50 Hz, 1 s)
3750 V AC (50 Hz, 60 s)
>900 V peak (type test) <sup>3</sup>
>700 V peak (type test)
>6 mm; cumulative, core floating
>5.5 mm; cumulative, core floating
>3 mm
>2.75 mm
>2 mm
P2 (to IEC 60664)
+155 °C (F) to (IEC 60085)
40/150/56 (to IEC 60068)
−25 °C +40 °C, humidity ≤75% RH
In accordance with JEDEC J-STD-020D T <sub>peak</sub> = +245 °C (T <sub>peak</sub> -5 °C for 30 seconds)
-40 °C +150 °C (component)
Approx. 2 g

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 $<sup>^3</sup>$  Partial discharge type test, refer to IEC 60664-1: Extinction voltage for basic and reinforced insulation ≥ V<sub>op peak</sub> x 1.2: 500 V x 1.2 = min. 600 V<sub>peak</sub>; Inception voltage for basic insulation ≥ V<sub>op</sub> x 1.5 = 500 V x 1.5 = min.750 V; Inception voltage for reinforced insulation ≥ V<sub>op</sub> x 1.875 = 300 V x 1.875 = min. 563 V<sub>peak</sub>



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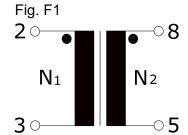
# Characteristics and ordering codes

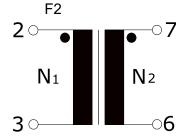
Topologies	Turns ratio N1/N2	L <sub>N1</sub>	Lleak,typ, <sub>N1</sub> μΗ	Isat, <sub>N1</sub> <sup>4</sup>	E*dt <sub>N1</sub> 5 (max, unipolar/ bipolar) µVs	$R_{DC,N1}$ $m\Omega$	$R_{DC,N2}$ $m\Omega$	Cp N1/N2	Fig.	Ordering code
B1, B2	1 : 1.08	≥ 100	0.35	-	15 / 30	350	410	9	F1	B78307A2276A003
B1, B2	1:0.76	≥ 100	0.45	-	18 / 36	360	300	9	F1	B78307A9741A003
B1, B2	1:3.67	≥ 10	0.1	-	10 / 20	200	700	6	F2	B78307A2385A003
B3,B4	1:4	2 ±10%	0.06	4	-	105	340	4	F3	B78307A2338A003 <sup>(3</sup>
B3,B4	4:1	25 ±10%	-	1	-	-	-	4	F4	B78307A2338A003 <sup>(3</sup>

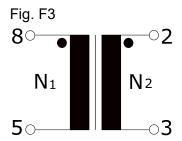
<sup>1)</sup> T≤150 °C, B= 200 mT, ΔB= 400 mT (bipolar mode). The maximum volt-sec rating limits the peak flux density to B= 200 mT when used in a unipolar drive application. For bipolar drive applications, a maximum volt-sec of two times is acceptable (\Delta B 400 mT).

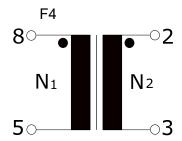
3) B78307A2238A003 Configuration 1 : 4 use pins 8-5 for primary; Configuration 4 : 1 use pins 2-3 for primary

# Circuit diagram









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<sup>&</sup>lt;sup>4</sup> T≤150 °C, L drop ≤20%

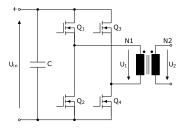
<sup>&</sup>lt;sup>5</sup> T≤150 °C,  $\widehat{B}$ = 200 mT,  $\Delta B$ = 400 mT (bipolar mode). The maximum volt-sec rating limits the peak flux density to  $\widehat{B}$ = 200 mT when used in a unipolar drive application. For bipolar drive applications, a maximum volt-sec of two times is acceptable (ΔB 400 mT)



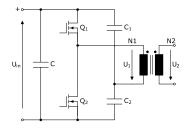
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# **Topology examples**

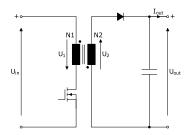
# B1) Full Bridge



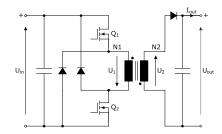
B2) Half Bridge



B3) Flyback



B4) Two switch flyback

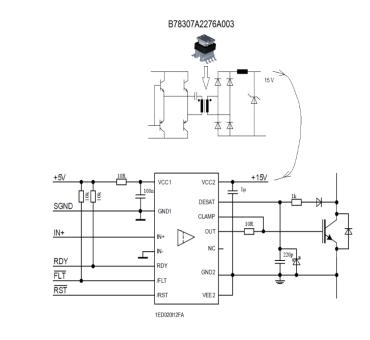


A1. Reference design for chipset Silicon Laboratory SiLab Si88xx Digital Isolator



Si88xx

A2. Reference design for chipset Infineon Driver IC 1ED020I12FA



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A2\_

A3

A4



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## Cautions and warnings

- Please note the recommendations in our Inductors data book (latest edition) and in the data sheets.
- Particular attention should be paid to the derating curves given there.
- The soldering conditions should also be observed. Temperatures quoted in relation to wave soldering refer to the pin, not the housing.
- If the components are to be washed varnished it is necessary to check whether the washing varnish agent that is used has a negative effect on the wire insulation, any plastics that are used, or on glued joints. In particular, it is possible for washing varnish agent residues to have a negative effect in the long-term on wire insulation. Washing processes may damage the product due to the possible static or cyclic mechanical loads (e.g. ultrasonic cleaning). They may cause cracks to develop on the product and its parts, which might lead to reduced reliability or lifetime.
- The following points must be observed if the components are potted in customer applications:
  - Many potting materials shrink as they harden. They therefore exert a pressure on the plastic housing or core. This pressure can have a deleterious effect on electrical properties, and in extreme cases can damage the core or plastic housing mechanically.
  - It is necessary to check whether the potting material used attacks or destroys the wire insulation, plastics or glue.
  - The effect of the potting material can change the high-frequency behaviour of the components.
  - Many coating materials have a negative effect (chemically and mechanically) on the winding wires, insulation materials and connecting points. Customers are always obligated to determine whether and to what extent their coating materials influence the component. Customers are responsible and bear all risk for the use of the coating material. TDK Electronics does not assume any liability for failures of our components that are caused by the coating material.
- Ceramics / ferrites are sensitive to direct impact. This can cause the core material to flake, or lead to breakage of the core.
- Even for customer-specific products, conclusive validation of the component in the circuit can only be carried out by the customer.

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