IAM-20381

High Performance Automotive 3-Axis MotionTracking Accelerometer

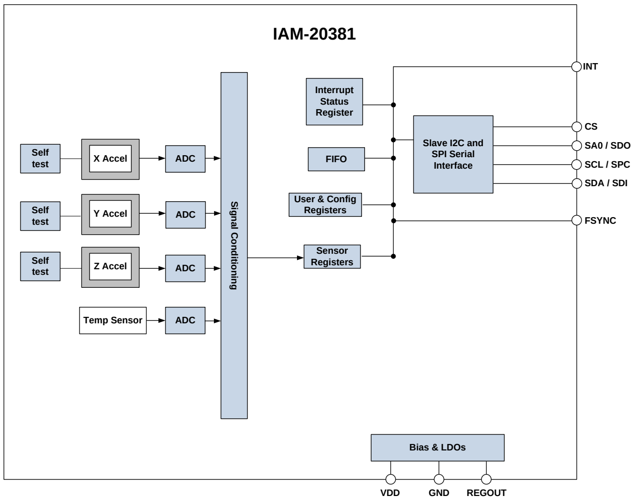
GENERAL DESCRIPTION

The IAM-20381 is a 3-axis MotionTracking accelerometer for Automotive applications in a small 3x3x0.75 mm^3 (16-pin LGA) package. It also features a 512-byte FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. IAM-20381, with its 3-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

BLOCK DIAGRAM



APPLICATIONS

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detections
- Accurate Location for Vehicle to Vehicle and Infrastructure
- 360º View Camera Stabilization
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

ORDERING INFORMATION

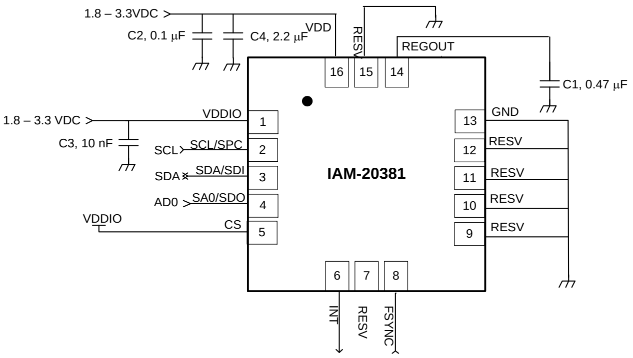
PART	AXES	TEMP RANGE	PACKAGE	MSL*
IAM-20381†	X,Y,Z	-40°C to +85°C	16-Pin LGA	3

†Denotes RoHS and Green-compliant package
* Moisture sensitivity level of the package

FEATURES

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g* and integrated 16-bit ADCs
- User-programmable digital filters for accelerometer, and temperature sensor
- Self-test
- Wake-on-motion interrupt for low power operation of applications processor
- Reliability testing performed according to AEC–Q100
    - PPAP and qualification data available upon request

TYPICAL OPERATING CIRCUIT



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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing description, specifications, and design related information on the IAM-20381 Automotive MotionTracking device. The device is housed in a small 3x3x0.75 mm^3 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The IAM-20381 is a 3-axis MotionTracking accelerometer for Automotive applications, in a small 3x3x0.75 mm^3 (16-pin LGA) package. It also features a 512-byte FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. IAM-20381, with its 3-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using either I^{2}C at 400 kHz or SPI at 8 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK-InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75 mm^3 (16-pin LGA), to provide a very small yet high-performance, low-cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detections
- Accurate Location for Vehicle to Vehicle and Infrastructure
- 360^o View Camera Stabilization
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

2 FEATURES

2.1 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in IAM-20381 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.2 ADDITIONAL FEATURES

The IAM-20381 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 3x3x0.75 mm^3 (16-pin LGA)
- 512-byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for accelerometer, and temperature sensor
- 10,000*g* shock tolerant
- 400 kHz Fast Mode I^{2}C for communicating with all registers
- 8 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, Full Scale = 8*g*, Low-Noise Mode enabled unless otherwise noted.

All Zero-g output, sensitivity, and noise specifications include board soldering effects.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	AFS_SEL=0		±2		*g*	3
	AFS_SEL=1		±4		*g*	3
	AFS_SEL=2		±8		*g*	3
	AFS_SEL=3		±16		*g*	3
ADC Word Length	Output in two's complement format		16		bits	3
Sensitivity Scale Factor	AFS_SEL=0		16,384		LSB/*g*	3
	AFS_SEL=1		8,192		LSB/*g*	3
	AFS_SEL=2		4,096		LSB/*g*	3
	AFS_SEL=3		2,048		LSB/*g*	3
Nonlinearity	Best Fit Straight Line for 2g, 25°C	-0.25		+0.25	%	1
Cross-Axis Sensitivity	25°C		±5		%	1
ZERO-G OUTPUT						
Initial Tolerance	All axes, 25°C		±50		m*g*	1
Zero-G Level Change vs. Temperature	-40°C to +85°C		±50		m*g*	1
NOISE PERFORMANCE						
Power Spectral Density	Low noise mode, -40°C to +85°C		135		µg/√Hz	1,4
	Low noise mode, -40°C to +85°C, including lifetime drift		190		µg/√Hz	1,4
Low Pass Filter Response	Programmable Range	5		218	Hz	3
Accelerometer Startup Time	From Sleep mode			20	ms	1
	From Cold Start, 1ms V_{DD} ramp			30	ms	1
Output Data Rate	Low power (duty-cycled)	0.24		500	Hz	1
	Low noise (active)	4		4000	Hz	

Table 1. Accelerometer Specifications

Please contact TDK-InvenSense for a datasheet with maximum and minimum performance values over temperature and lifetime.

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.

3.2 ELECTRICAL SPECIFICATIONS

3.2.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS & BOOT TIME						
Normal Mode	3-axis Accelerometer, 4 kHz ODR		390		µA	1
Accelerometer Low -Power Mode	100 Hz ODR, 1x averaging		57		µA	2
Full-Chip Sleep Mode			6		µA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 2. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Based on simulation.

3.2.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Room Temperature Offset	25°C		0		°C	1
Sensitivity	Untrimmed		326.8		LSB/°C	1
POWER-ON RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
	From sleep			5	ms	1
I^2C ADDRESS	SA0 = 0 SA0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I^2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5 V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	

INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3 SMPLRT_DIV=0		32		kHz	2
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6	-10		+10	%	1
	CLK_SEL=1,2,3,4,5	-1		+1	%	1

Table 3. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.

3.2.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	1
	High Speed Characterization		1	8	MHz	1, 2
SPI Modes			Modes 0 and 3			
I^{2}C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 4. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 8MHz operation.

3.3 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF	$20+0.1C_b$		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF	$20+0.1C_b$		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

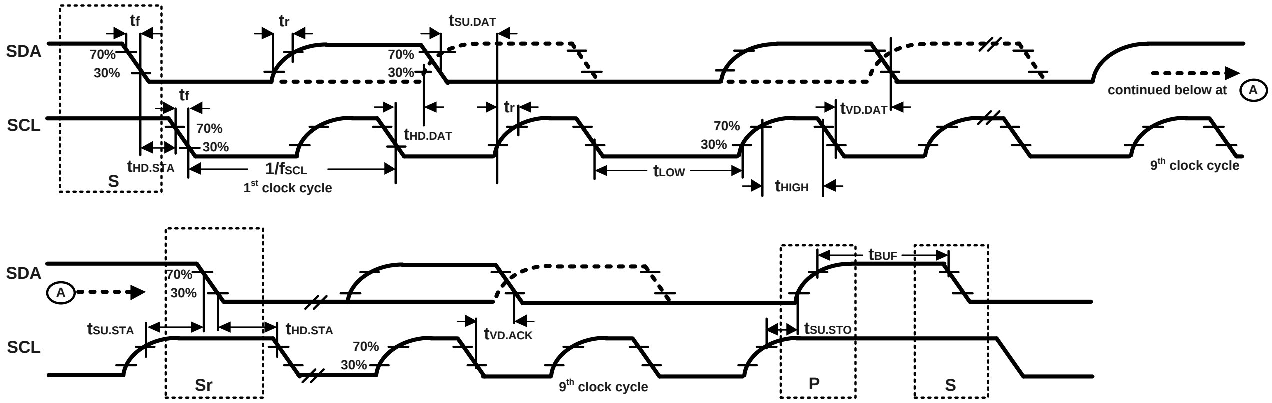


Figure 1. I²C Bus Timing Diagram

3.4 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A = 25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SPC Clock Frequency				8	MHz	1
t_{LOW}, SPC Low Period		56			ns	1
t_{HIGH}, SPC High Period		56			ns	1
$t_{SU.CS}$, CS Setup Time		2			ns	1
$t_{HD.CS}$, CS Hold Time		63			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			40	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	6			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1
t_{Fall}, SCLK Fall Time				6.5	ns	2
t_{Rise}, SCLK Rise Time				6.5	ns	2

Table 6. SPI Timing Characteristics (8 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Based on other parameter values.

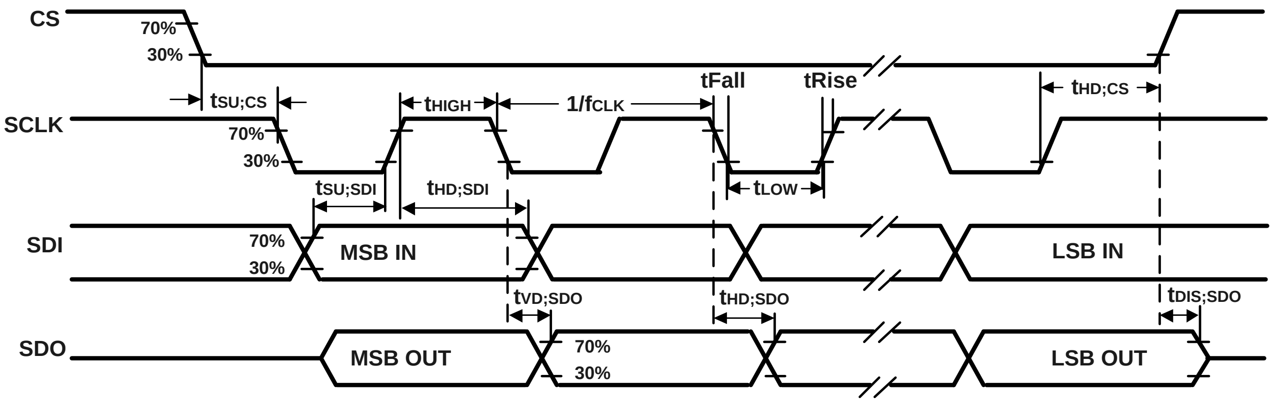


Figure 2. SPI Bus Timing Diagram

3.5 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to 4V
Supply Voltage, VDDIO	-0.5V to 4V
REGOUT	-0.5V to 2V
Input Voltage Level (SA0, FSYNC, SCL, SDA)	-0.5V to VDDIO + 0.5V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2 ms
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-40°C to 125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 750V (CDM Corner Pins) 500V (CDM All Other Pins)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 7. Absolute Maximum Ratings

3.6 THERMAL INFORMATION

THERMAL METRIC	DESCRIPTION	VALUE
θ_{JA}	Junction-to-ambient thermal resistance	84.58 °C/W
ψ_{JT}	Junction-to-top characterization parameter	7 °C/W

Table 8. Thermal Information

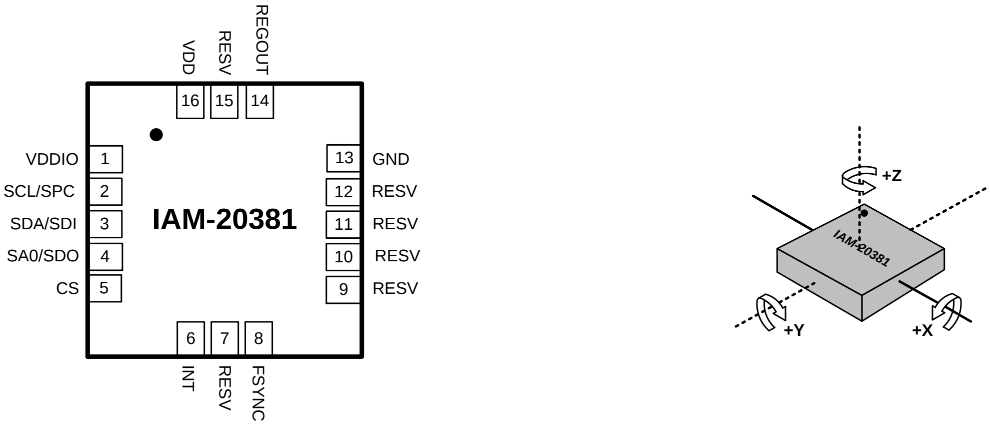
4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage
2	SCL/SPC	I^{2}C serial clock (SCL); SPI serial clock (SPC)
3	SDA/SDI	I^{2}C serial data (SDA); SPI serial data input (SDI)
4	SA0/SDO	I^{2}C slave address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I^{2}C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused
9	RESV	Reserved. Connect to GND
10	RESV	Reserved. Connect to GND
11	RESV	Reserved. Connect to GND
12	RESV	Reserved. Connect to GND
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND
16	VDD	Power Supply

Table 9. Signal Descriptions

Note: If power up is performed with both SCL/SPC and CS pins held low a software reset is required using the PWR_MGMT_1 register, prior to initialization. Please refer to sections 4.17 for detailed power-up instructions.



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and thickness

Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for IAM-20381 3.0x3.0x0.75 mm^3 LGA

4.2 TYPICAL OPERATING CIRCUIT

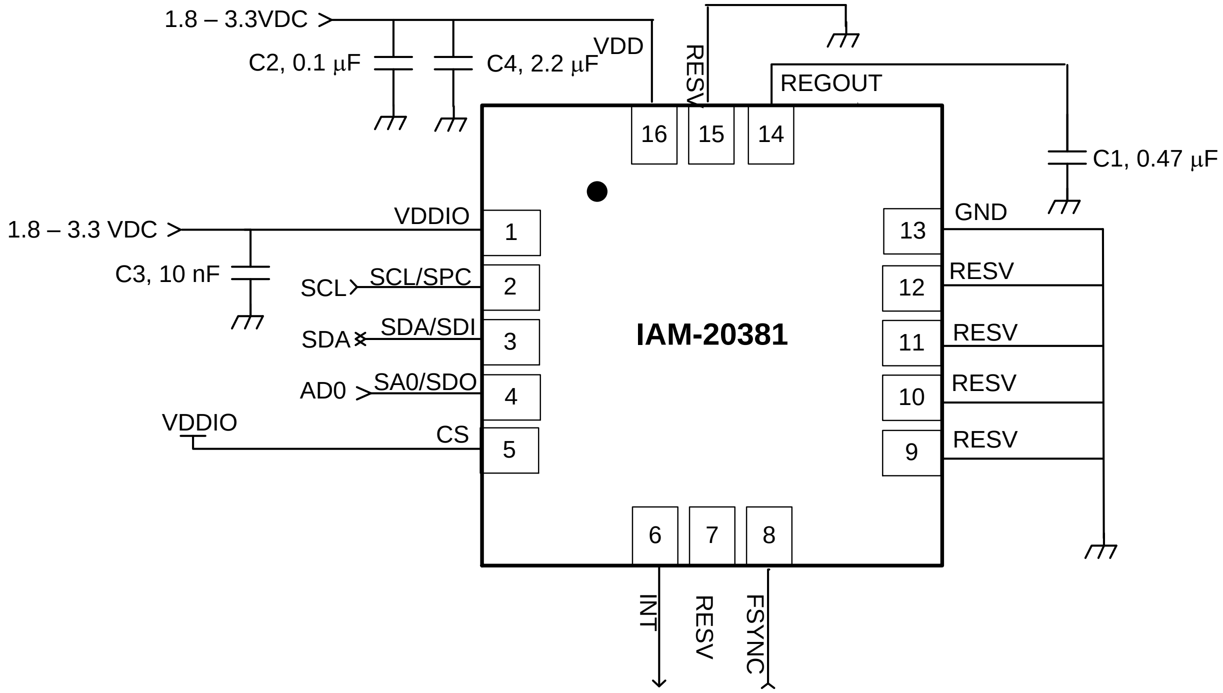


Figure 4. IAM-20381 LGA Application Schematic

Note: I²C lines are open drain and pullup resistors (e.g. 10 kΩ) are required.

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	X7R, 0.47 µF ±10%	1
VDD Bypass Capacitors	C2	X7R, 0.1 µF ±10%	1
	C4	X7R, 2.2 µF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10 nF ±10%	1

Table 10. Bill of Materials

4.4 BLOCK DIAGRAM

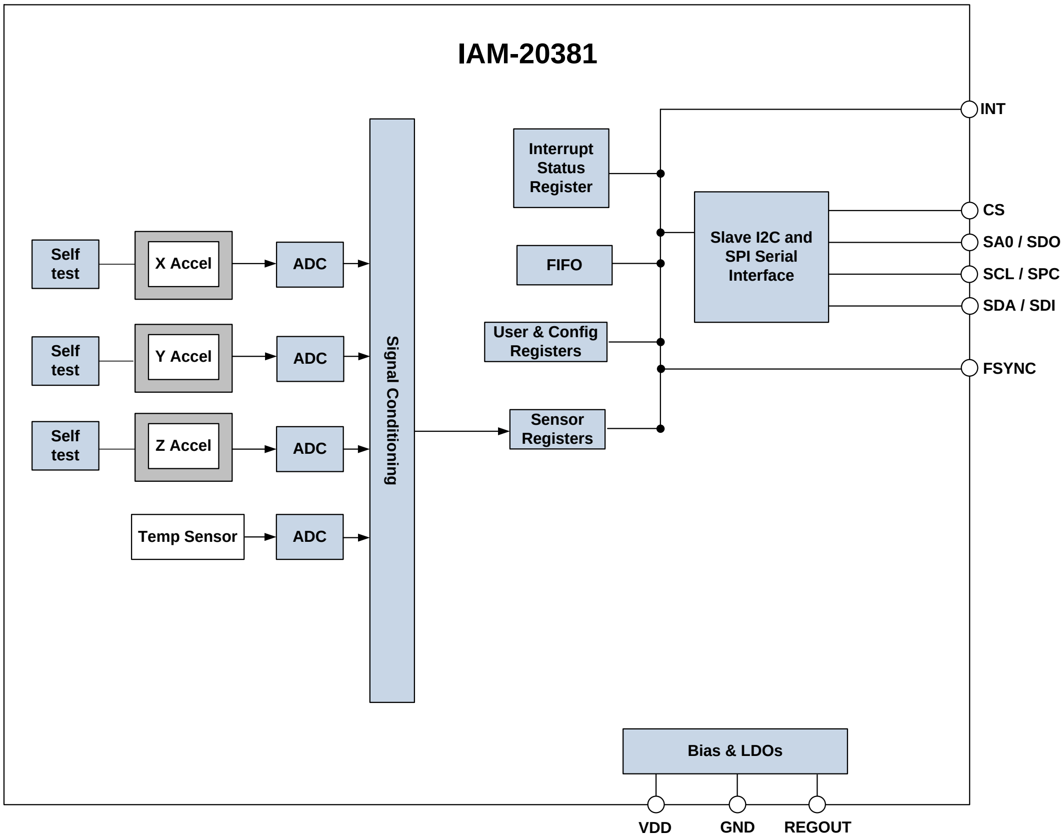


Figure 5. IAM-20381 Block Diagram

4.5 OVERVIEW

The IAM-20381 is comprised of the following key blocks and functions:

- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^{2}C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20381's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The IAM-20381's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.7 I^{2}C AND SPI SERIAL COMMUNICATIONS INTERFACES

The IAM-20381 communicates to a system processor using either a SPI or an I^{2}C serial interface. The IAM-20381 always acts as a slave when communicating to the system processor. The LSB of the I^{2}C slave address is set by pin 4 (SA0).

4.7.1 IAM-20381 Solution Using I^{2}C Interface

In Figure 6, the system processor is an I^{2}C master to the IAM-20381.

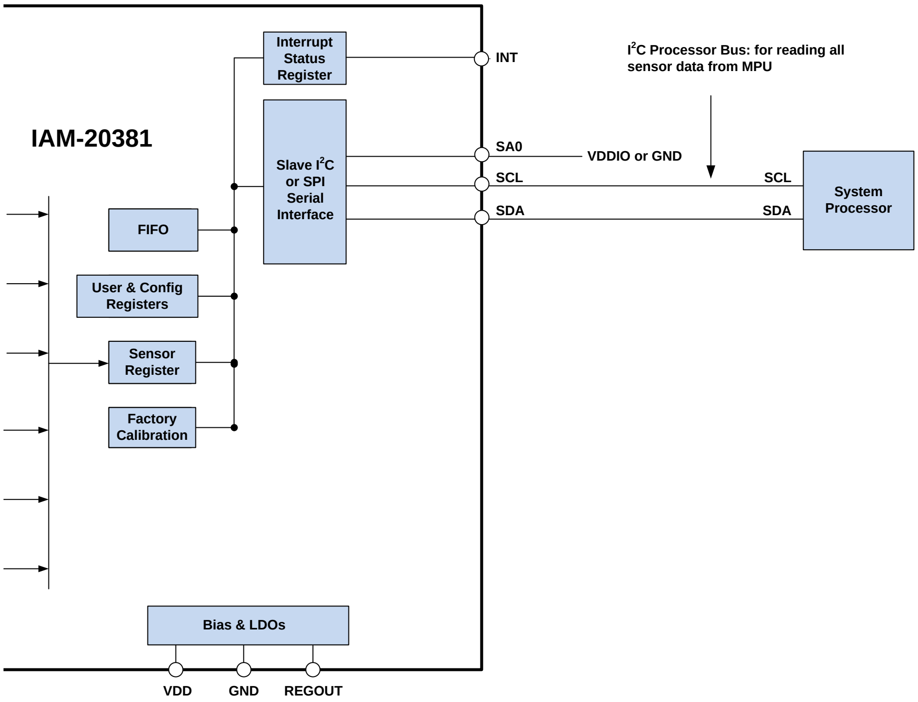


Figure 6. IAM-20381 Solution Using I^{2}C Interface

4.7.2 IAM-20381 Solution Using SPI Interface

In Figure 7, the system processor is an SPI master to the IAM-20381. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

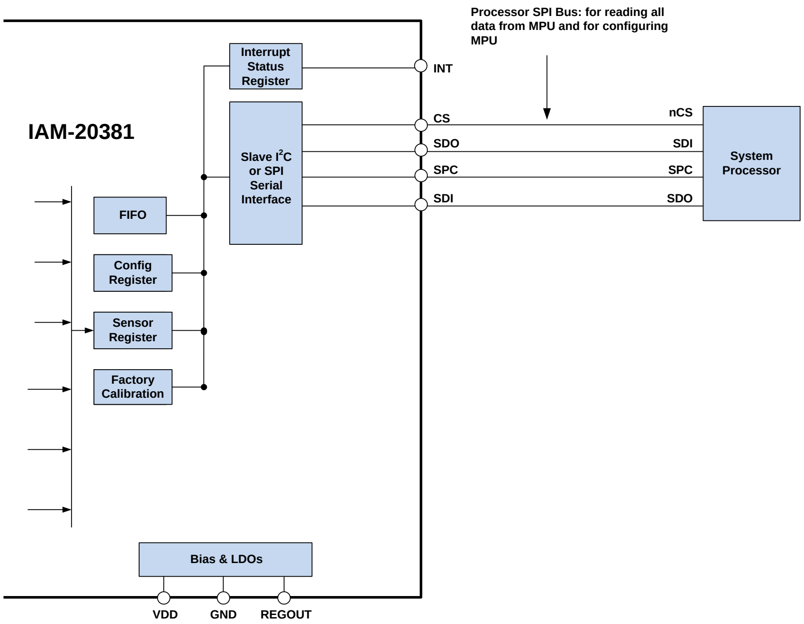


Figure 7. IAM-20381 Solution Using SPI Interface

4.8 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the accelerometer self-test register (register 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.9 CLOCKING

The IAM-20381 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.10 SENSOR DATA REGISTERS

The sensor data registers contain the latest accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.11 FIFO

The IAM-20381 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data are written into the FIFO. Possible choices include accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data are available.

The IAM-20381 allows FIFO read in low-power accelerometer mode.

4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are new data are available to be read (from the FIFO and Data registers), FIFO overflow and wake on motion (WoM). The interrupt status can be read from the Interrupt Status register.

4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the IAM-20381 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IAM-20381. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.16 STANDARD POWER MODES

Table 11 lists the user-accessible power modes for IAM-20381.

MODE	NAME	ACCEL
1	Sleep Mode	Off
3	Accelerometer Low-Power Mode	Duty-Cycled
4	Accelerometer Low-Noise Mode	On

Table 11. Standard Power Modes for IAM-20381

Notes:

1. Power consumption for individual modes can be found in section 3.2.1.

4.17 SENSOR INITIALIZATION AND BASIC CONFIGURATION

The basic configuration of the IAM-20381 includes the following steps:

- Power-up sequence
- Sensor initialization and clock source selection
- Digital interface access test
- Output data rate (i.e. sampling frequency) selection
- Full scale range selection
- Filter frequency selection
- Power mode selection

4.17.1 Power-up sequence

When applying VDD, the power voltage ramp is detected and a power-on-reset sequence is triggered inside the component. During this phase the device starts operating and internal logic levels are defined. For proper component initialization the power-up should be performed ensuring that CS and SCL pins are not in an undetermined state during the VDD ramp. Power-up should be performed with SCL/SPC low, power-up with SCL/SPC high is not a supported case and must be avoided.

It is worth noting that if the I/O pins (e.g. CS, SCL/SPC) are between V_{IL} and V_{IH} when the power-on-reset sequence is triggered, their value is undetermined and the internal logic levels may not be properly defined. It should also be noted that V_{IL} and V_{IH} are related to VDDIO and their value changes at power-up according to the applied VDDIO voltage ramp.

Power-up sequences that do not respect the conditions above may not lead to proper digital interface initialization. In this case a preliminary soft reset operation (PWR_MGMT_1 register set 0x81) must be performed to reset the digital interface, as soon as both VDD and VDDIO are stable at their final voltage. Since the digital interface may not be properly initialized, the device may not provide the acknowledge signal if the I^2C protocol is used.

4.17.2 Sensor Initialization and Clock Source Selection

When power-up sequence is completed, a soft reset is required to initialize the sensor and let the IAM-20381 select the best clock source. The soft reset must be performed by setting the register PWR_MGMT_1 (address 0x6B) to 0x81 (see section 9.18), prior to registers initialization.

Soft reset must be performed as first operation after the power-up sequence to ensure the proper component registers setting. Correct WHO_AM_I value is ensured only after that soft reset has been completed.

4.17.3 Digital interface access test

When soft reset is completed, make sure the component registers access can be done as expected. WHO_AM_I (address 0x75) register can be used for this purpose to verify the identity of the device.

4.17.4 Output Data Rate Selection

To set the output data rate (ODR) to the desired frequency, select the sample rate divider by setting the register SMPLRT_DIV (address 0x19) to the desired value (see section 9.2). For instance, to set the output data rate to 100 Hz, write 0x09 into SMPLRT_DIV.

4.17.5 Full Scale Range Selection

To set the full-scale range (FSR) of the accelerometer, set the register ACCEL_CONFIG (address 0x1C) to the desired value (see section 9.4). For instance, to set the FSR of the accelerometer to 2g, write 0x00 into ACCEL_CONFIG.

4.17.6 Filter Selection

To set the corner frequency of the digital low-pass filter (DLPF) of the accelerometer, set the register ACCEL_CONFIG2 (address 0x1D) to the desired value (see section 9.5) For instance, to set the corner frequency of the DLPF of the accelerometer to 10.2 Hz, write 0x05 into ACCEL_CONFIG2.

5 PROGRAMMABLE INTERRUPTS

The IAM-20381 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

INTERRUPT NAME	MODULE
Motion Detection	Motion
FIFO Overflow	FIFO
Data Ready	Sensor Registers

Table 12. Table of Interrupt Sources

5.1 WAKE-ON-MOTION INTERRUPT

The IAM-20381 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 0, SLEEP = 0

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = b111

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_INT_EN[2:0] = b111 to enable motion interrupt

Once triggered, WoM interrupt is generated on INT pin

Step 4: Set Motion Threshold

- Set the motion threshold in ACCEL_WOM_THR register (0x1F)

Step 5: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = 1 to enable the Wake-on-Motion detection logic
- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_MODE = 1 to make the detection insensitive to the acceleration DC-component (Compare the current sample with the previous sample).
- In ACCEL_INTEL_CTRL register (0x69) ensure that bit 0 is set to 0.

Step 6: Set Accelerometer WoM ODR Selection

- In LP_MODE_CFG register (0x1E) set ACCEL_WOM_ODR_CTRL[3:0] according to Table 17

Step 7: Enable Cycle Mode (Accelerometer WoM Mode)

- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0
- In PWR_MGMT_1 register (0x6B) set ACCEL_CYCLE = 1

6 DIGITAL INTERFACE

6.1 I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the IAM-20381 can be accessed using either I^{2}C at 400 kHz or SPI at 8 MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage.
4	SA0 / SDO	I^{2}C Slave Address LSB (SA0); SPI serial data output (SDO)
2	SCL / SPC	I^{2}C serial clock (SCL); SPI serial clock (SPC)
3	SDA / SDI	I^{2}C serial data (SDA); SPI serial data input (SDI)

Table 13. Serial Interface

Note: To prevent switching into I^{2}C mode when using SPI, the I^{2}C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the “Start-Up Time for Register Read/Write” in section 3.2.2.

For further information regarding the I2C_IF_DIS bit, please refer to sections 8 and 9 of this document.

6.2 I^{2}C INTERFACE

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IAM-20381 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the IAM-20381 is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin SA0. This allows two IAM-20381s to be connected to the same I^{2}C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

6.3 IC COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I^{2}C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see Figure 8).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

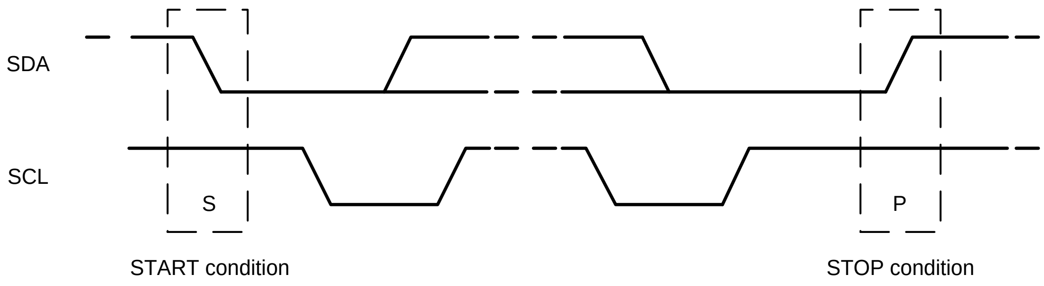


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I^{2}C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to Figure 9).

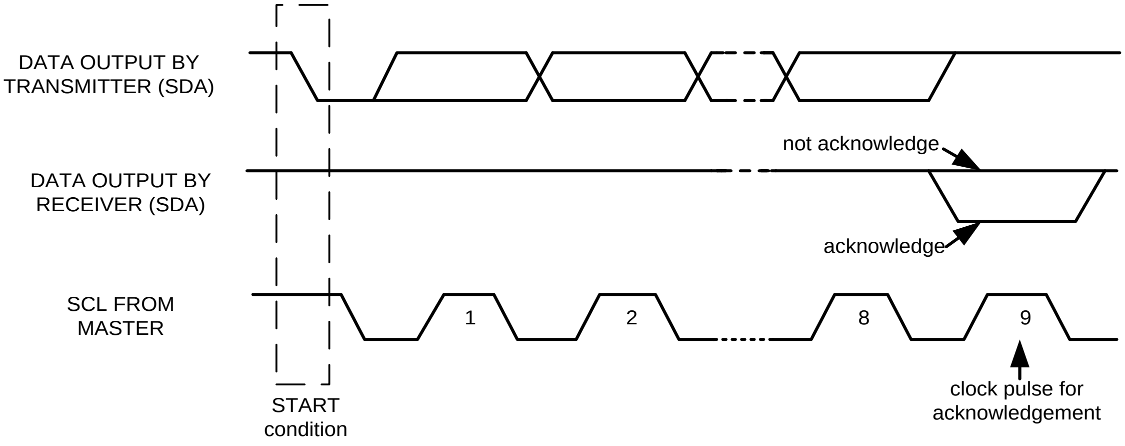


Figure 9. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

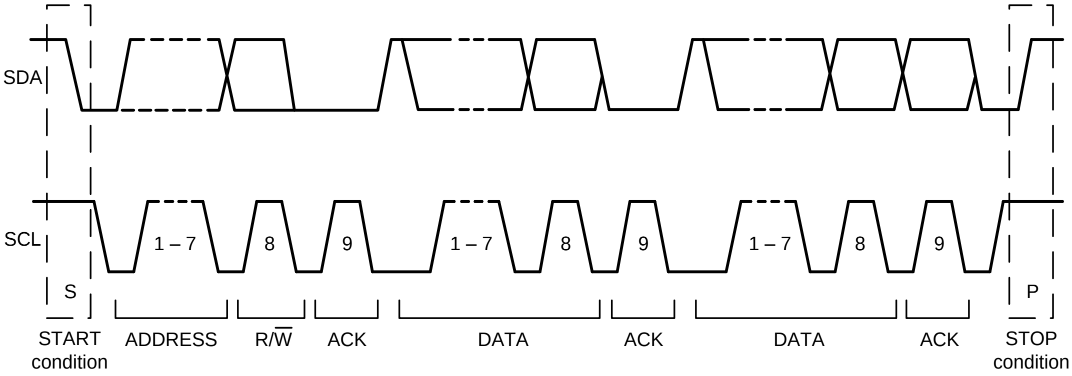


Figure 10. Complete I²C Data Transfer

To write the internal IAM-20381 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the IAM-20381 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IAM-20381 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IAM-20381 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal IAM-20381 registers, the master sends a start condition, followed by the I^{2}C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IAM-20381, the master transmits a start signal followed by the slave address and read bit. As a result, the IAM-20381 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I^{2}C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^{2}C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	IAM-20381 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 14. I^{2}C Terms

6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The IAM-20381 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SPC), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data are delivered MSB first and LSB last
2. Data are latched on the rising edge of SPC
3. Data should be transitioned on the falling edge of SPC
4. The maximum frequency of SPC is 8 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data are two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

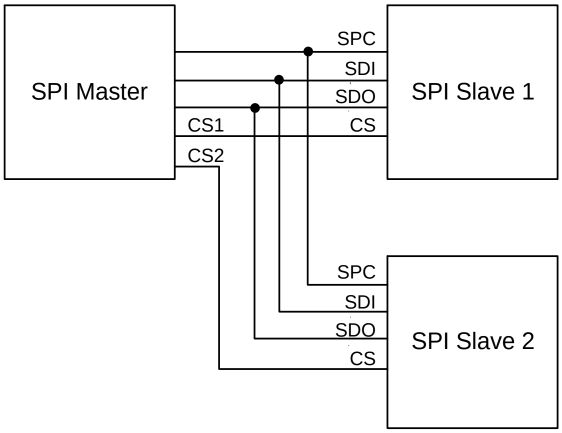


Figure 11. Typical SPI Master/Slave Configuration

7 SERIAL INTERFACE CONSIDERATIONS

7.1 IAM-20381 SUPPORTED INTERFACES

The IAM-20381 supports I^{2}C communications on its serial interface.

The IAM-20381's I/O logic levels are set to be VDDIO.

Figure 12 depicts a sample circuit of IAM-20381. It shows the relevant logic levels and voltage connections.

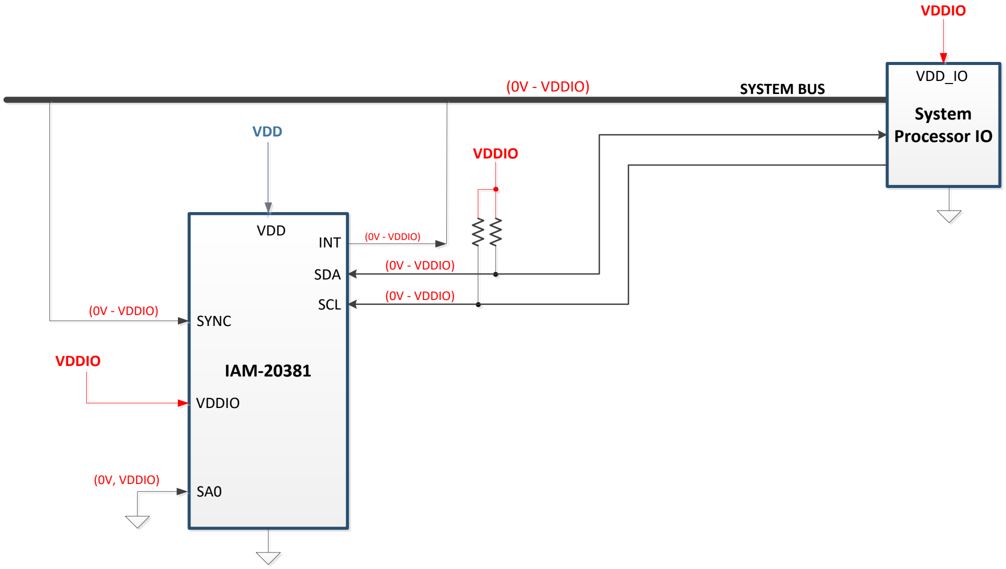


Figure 12. I/O Levels and Connections

8 REGISTER MAP

The following table lists the register map for the IAM-20381.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Accessible (writable) in Sleep Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D	13	SELF_TEST_X_ACCEL	R/W	N	XA_ST_DATA[7:0]							
0E	14	SELF_TEST_Y_ACCEL	R/W	N	YA_ST_DATA[7:0]							
0F	15	SELF_TEST_Z_ACCEL	R/W	N	ZA_ST_DATA[7:0]							
19	25	SMPLRT_DIV	R/W	N	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	N	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1C	28	ACCEL_CONFIG	R/W	N	XA_ST	YA_ST	ZA_ST	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	R/W	N	-		DEC2_CFG[1:0]		ACCEL_FCHOICE_B	A_DLPF_CFG[2:0]		
1E	30	LP_MODE_CFG	R/W	N					ACCEL_WOM_ODR_CTRL [3:0]			
1F	31	ACCEL_WOM_THR	R/W	N	WOM_THR[7:0]							
23	35	FIFO_EN	R/W	N	TEMP_FIFO_EN	-	-	-	ACCEL_FIFO_EN	-	-	-
36	54	FSYNC_INT	R/C	N	FSYNC_INT	-	-	-	-	-	-	-
37	55	INT_PIN_CFG	R/W	Y	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	FSYNC_INT_LEVEL	FSYNC_INT_MODE_EN	-	-
38	56	INT_ENABLE	R/W	Y	WOM_INT_EN[7:5]			FIFO_OFLOW_EN	-	-	-	DATA_RDY_INT_EN
3A	58	INT_STATUS	R/C	N	WOM_INT[7:5]			FIFO_OFLOW_INT	-	-	-	DATA_RDY_INT
3B	59	ACCEL_XOUT_H	R	N	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	R	N	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	R	N	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	R	N	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	R	N	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	R	N	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	R	N	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	N	TEMP_OUT[7:0]							
68	104	SIGNAL_PATH_RESET	R/W	N	-	-	-	-	-	-	ACCEL_RST	TEMP_RST
69	105	ACCEL_INTEL_CTRL	R/W	N	ACCEL_INTEL_EN	ACCEL_INTEL_MODE	-					
6A	106	USER_CTRL	R/W	N	-	FIFO_EN	-	I2C_IF_DIS	-	FIFO_RST	-	SIG_COND_RST
6B	107	PWR_MGMT_1	R/W	Y	DEVICE_RESET	SLEEP	ACCEL_CYCLE	-	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	R/W	Y	FIFO_LP_EN	-	STBY_XA	STBY_YA	STBY_ZA	-	-	-
72	114	FIFO_COUNTH	R	N	-			FIFO_COUNT[12:8]				
73	115	FIFO_COUNTL	R	N	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	R/W	N	FIFO_DATA[7:0]							
75	117	WHO_AM_I	R	N	WHOAMI[7:0]							
77	119	XA_OFFSET_H	R/W	N	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	R/W	N	XA_OFFS [6:0]							-
7A	122	YA_OFFSET_H	R/W	N	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	R/W	N	YA_OFFS [6:0]							-
7D	125	ZA_OFFSET_H	R/W	N	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	R/W	N	ZA_OFFS [6:0]							-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below, also the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Self-test registers 13, 14, 15 contain pre-programmed values
- Register 107 (0x40) Power Management 1 = 0x01
- Register 117 (0xB6) WHO_AM_I (default value is reported in section 9.22)
- Registers 119, 120, 122, 123, 125, 126 contain pre-programmed offset cancellation values

9 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the IAM-20381.

Note: The device will come up in Low Noise mode upon power-up.

9.1 REGISTERS 13 TO 15 – ACCELEROMETER SELF-TEST REGISTERS

Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL

Type: READ/WRITE

Register Address: 13, 14, 15 (Decimal); 0D, 0E, 0F (Hex)

REGISTER	BITS	NAME	FUNCTION
SELF_TEST_X_ACCEL	[7:0]	XA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_ACCEL	[7:0]	YA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_ACCEL	[7:0]	ZA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620 / 2^{FS}) * 1.01^{(ST\_code - 1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full-Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in TDK-InvenSense’s factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC / (2620 / 2^{FS}))}{\log(1.01)}\right) + 1$$

9.2 REGISTER 25 – SAMPLE RATE DIVIDER

Register Name: SMPLRT_DIV

Register Type: READ/WRITE

Register Address: 25 (Decimal); 19 (Hex)

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. **Note**: This register is only effective when FCHOICE_B register bits are 2’b00, and (0 < DLPF_CFG < 7). This is the update rate of the sensor register: SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV) Where INTERNAL_SAMPLE_RATE = 1 kHz

9.3 REGISTER 26 – CONFIGURATION

Register Name: CONFIG

Register Type: READ/WRITE

Register Address: 26 (Decimal); 1A (Hex)

BIT	NAME	FUNCTION
[7]	-	Always set to 0.
[6]	FIFO_MODE	When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.
[5:3]	EXT_SYNC_SET[2:0]	Enables the FSYNC pin data to be sampled. EXT_SYNC_SET / FSYNC bit location: 0 – function disabled 1 – TEMP_OUT_L[0] 2 – Reserved 3 – Reserved 4 – Reserved 5 – ACCEL_XOUT_L[0] 6 – ACCEL_YOUT_L[0] 7 – ACCEL_ZOUT_L[0] FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.
[2:0]	DLPF_CFG[2:0]	For the DLPF to be used, FCHOICE_B[1:0] is 2'b00. See Table 15.

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The temperature sensor data is filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in Table 15

FCHOICE_B		DLPF_CFG	Temperature Sensor
<1>	<0>		3-dB BW (Hz)
X	1	X	4000
1	0	X	4000
0	0	0	4000
0	0	1	188
0	0	2	98
0	0	3	42
0	0	4	20
0	0	5	10
0	0	6	5
0	0	7	4000

Table 15. Temperature Sensor Bandwidth Configuration

9.4 REGISTER 28 – ACCELEROMETER CONFIGURATION

Register Name: ACCEL_CONFIG

Register Type: READ/WRITE

Register Address: 28 (Decimal); 1C (Hex)

BIT	NAME	FUNCTION
[7]	XA_ST	X Accel self-test.
[6]	YA_ST	Y Accel self-test.
[5]	ZA_ST	Z Accel self-test.
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	-	Reserved.

9.5 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

Register Name: ACCEL_CONFIG2

Register Type: READ/WRITE

Register Address: 29 (Decimal); 1D (Hex)

BIT	NAME	FUNCTION
[7:6]	-	Reserved.
[5:4]	DEC2_CFG[1:0]	Averaging filter settings for Low Power Accelerometer mode: 0 = Average 4 samples 1 = Average 8 samples 2 = Average 16 samples 3 = Average 32 samples
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in Table 16.
[2:0]	A_DLPF_CFG	Accelerometer low pass filter setting as shown in Table 16.

ACCEL_FCHOICE_B	A_DLPF_CFG	Accelerometer		
		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)
1	X	1046.0	1100.0	4
0	0	218.1	235.0	1
0	1	218.1	235.0	1
0	2	99.0	121.3	1
0	3	44.8	61.5	1
0	4	21.2	31.0	1
0	5	10.2	15.5	1
0	6	5.1	7.8	1
0	7	420.0	441.6	1

Table 16. Accelerometer Data Rates and Bandwidths (Low Noise Mode)

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the low-noise mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K.

Table 17 lists the accelerometer filter bandwidths, noise, and current consumption available in the low-power mode of operation. In the low-power mode of operation, the accelerometer is duty-cycled.

ACCEL_FCHOICE_B		1	0	0	0	0
A_DLPF_CFG		x	7	7	7	7
DEC2_CFG		x	0	1	2	3
Averages		1x	4x	8x	16x	32x
Ton (ms)		1.084	1.84	2.84	4.84	8.84
Noise BW (Hz)		1100.0	441.6	235.4	121.3	61.5
Noise (mg) TYP based on 250 µg/√Hz		8.3	5.3	3.8	2.8	2.0
ACCEL_WOM_ODR_CTRL	**ODR (Hz)**	**Current Consumption (µA) TYP**				
4	3.9	8.4	9.4	10.8	13.6	19.2
5	7.8	9.8	11.9	14.7	20.3	31.4
6	15.6	12.8	17.0	22.5	33.7	55.9
7	31.3	18.7	27.1	38.2	60.4	104.9
8	62.5	30.4	47.2	69.4	113.9	202.8
9	125.0	57.4	87.5	132.0	220.9	N/A
10	250.0	100.9	168.1	257.0	N/A	
11	500.0	194.9	329.3	N/A		

Table 17. Accelerometer Filter Bandwidths, Noise, and Current Consumption (Low-Power Mode)

9.6 REGISTER 30 – LOW POWER MODE CONFIGURATION

Register Name: LP_MODE_CFG

Register Type: READ/WRITE

Register Address: 30 (Decimal); 1E (Hex)

BIT	NAME	FUNCTION
[7:4]	G_AVGCFG[2:0]	Reserved
[3:0]	ACCEL_WOM_ODR_CTRL[3:0]	Accelerometer WoM Mode ODR configuration. ACCEL_WOM_ODR_CTRL is effective only when ACCEL_CYCLE is set to '1': 0 to 3 = RESERVED 4 = 3.9 Hz 5 = 7.8 Hz 6 = 15.6 Hz 7 = 31.3 Hz 8 = 62.5 Hz 9 = 125 Hz 10 = 250 Hz 11 = 500 Hz 12 to 15 = RESERVED

9.7 REGISTER 31 – WAKE-ON MOTION THRESHOLD (ACCELEROMETER)

Register Name: ACCEL_WOM_THR

Register Type: READ/WRITE

Register Address: 31 (Decimal); 1F (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_THR[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for accelerometer. Wake on motion threshold resolution is 4 mg/LSB regardless the selected full scale.

9.8 REGISTER 35 – FIFO ENABLE

Register Name: FIFO_EN

Register Type: READ/WRITE

Register Address: 35 (Decimal); 23 (Hex)

BIT	NAME	FUNCTION
[7]	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate. 0 – Function is disabled.
[6:4]	-	Reserved.
[3]	ACCEL_FIFO_EN	1 – Write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
[2:0]	-	Reserved.

9.9 REGISTER 54 – FSYNC INTERRUPT STATUS

Register Name: FSYNC_INT

Register Type: READ to CLEAR

Register Address: 54 (Decimal); 36 (Hex)

BIT	NAME	FUNCTION
[7]	FSYNC_INT	This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read.

9.10 REGISTER 55 – INT/DRDY PIN / BYPASS ENABLE CONFIGURATION

Register Name: INT_PIN_CFG

Register Type: READ/WRITE

Register Address: 55 (Decimal); 37 (Hex)

BIT	NAME	FUNCTION
[7]	INT_LEVEL	1 – The logic level for INT/DRDY pin is active low. 0 – The logic level for INT/DRDY pin is active high.
[6]	INT_OPEN	1 – INT/DRDY pin is configured as open drain. 0 – INT/DRDY pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT/DRDY pin level held until interrupt status is cleared. 0 – INT/DRDY pin indicates interrupt pulse's width is 50 µs.
[4]	INT_RD_CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
[3]	FSYNC_INT_LEVEL	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by *FSYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.
[1]	-	Reserved.
[0]	-	Always set to 0.

9.11 REGISTER 56 – INTERRUPT ENABLE

Register Name: INT_ENABLE

Register Type: READ/WRITE

Register Address: 56 (Decimal); 38 (Hex)

BIT	NAME	FUNCTION
[7:5]	WOM_INT_EN[7:5]	111 – Enable WoM interrupt on accelerometer. 000 – Disable WoM interrupt on accelerometer.
[4]	FIFO_OFLOW_EN	1 – Enables a FIFO buffer overflow to generate an interrupt. 0 – Function is disabled.
[3:1]	-	Reserved.
[0]	DATA_RDY_INT_EN	Data ready interrupt enable.

9.12 REGISTER 58 – INTERRUPT STATUS

Register Name: INT_STATUS

Register Type: READ to CLEAR

Register Address: 58 (Decimal); 3A (Hex)

BIT	NAME	FUNCTION
[7:5]	WOM_INT	Accelerometer WoM interrupt status. Cleared on Read. 111 – WoM interrupt on accelerometer
[4]	FIFO_OFLOW_INT	This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read.
[3:1]	-	Reserved.
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

9.13 REGISTERS 59 TO 64 – ACCELEROMETER MEASUREMENTS

Register Name: ACCEL_XOUT_H

Register Type: READ only

Register Address: 59 (Decimal); 3B (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_H[15:8]	High byte of accelerometer x-axis data.

Register Name: ACCEL_XOUT_L

Register Type: READ only

Register Address: 60 (Decimal); 3C (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_L[7:0]	Low byte of accelerometer x-axis data.

Register Name: ACCEL_YOUT_H

Register Type: READ only

Register Address: 61 (Decimal); 3D (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_H[15:8]	High byte of accelerometer y-axis data.

Register Name: ACCEL_YOUT_L

Register Type: READ only

Register Address: 62 (Decimal); 3E (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_L[7:0]	Low byte of accelerometer y-axis data.

Register Name: ACCEL_ZOUT_H

Register Type: READ only

Register Address: 63 (Decimal); 3F (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_H[15:8]	High byte of accelerometer z-axis data.

Register Name: ACCEL_ZOUT_L

Register Type: READ only

Register Address: 64 (Decimal); 40 (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_L[7:0]	Low byte of accelerometer z-axis data.

9.14 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

Register Name: TEMP_OUT_H

Register Type: READ only

Register Address: 65 (Decimal); 41 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[15:8]	High byte of the temperature sensor output.

Register Name: TEMP_OUT_L

Register Type: READ only

Register Address: 66 (Decimal); 42 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[7:0]	Low byte of the temperature sensor output. **TEMP_degC** = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25degC

9.15 REGISTER 104 – SIGNAL PATH RESET

Register Name: SIGNAL_PATH_RESET

Register Type: READ/WRITE

Register Address: 104 (Decimal); 68 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved.
[1]	ACCEL_RST	Reset accel digital signal path. **Note**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. **Note**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

9.16 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

Register Name: ACCEL_INTEL_CTRL

Register Type: READ/WRITE

Register Address: 105 (Decimal); 69 (Hex)

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic.
[6]	ACCEL_INTEL_MODE	0 – Do not use. 1 – Compare the current sample with the previous sample.
[5:0]	**-**	Reserved.

9.17 REGISTER 106 – USER CONTROL

Register Name: USER_CTRL

Register Type: READ/WRITE

Register Address: 106 (Decimal); 6A (Hex)

BIT	NAME	FUNCTION
[7]	**-**	Reserved.
[6]	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register.
[5]	-	Reserved.
[4]	I2C_IF_DIS	1 – Disable I²C Slave module and put the serial interface in SPI mode only.
[3]	**-**	Reserved.
[2]	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
[1]	-	Reserved.
[0]	SIG_COND_RST	1 – Reset all accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

9.18 REGISTER 107 – POWER MANAGEMENT 1

Register Name: PWR_MGMT_1

Register Type: READ/WRITE

Register Address: 107 (Decimal); 6B (Hex)

BIT	NAME	FUNCTION
[7]	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done.
[6]	SLEEP	When set to 1, the chip is set to sleep mode. Default setting is 0.
[5]	ACCEL_CYCLE	When set to 1, and SLEEP and STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample at a rate determined by SMPLRT_DIV. **Note**: When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	-	Reserved.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
[2:0]	CLKSEL[2:0]	**Code** **Clock Source** 0 Internal 20 MHz oscillator. 1 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 2 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 3 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 4 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 Internal 20 MHz oscillator. 7 Stops the clock and keeps timing generator in reset.

Note: The default value of CLKSEL[2:0] is 001.

9.19 REGISTER 108 – POWER MANAGEMENT 2

Register Name: PWR_MGMT_2

Register Type: READ/WRITE

Register Address: 108 (Decimal); 6C (Hex)

BIT	NAME	FUNCTION
[7]	FIFO_LP_EN	1 – Enable FIFO in low-power accelerometer mode. Default setting is 0.
[6]	-	Reserved.
[5]	STBY_XA	1 – X accelerometer is disabled. 0 – X accelerometer is on.
[4]	STBY_YA	1 – Y accelerometer is disabled. 0 – Y accelerometer is on.
[3]	STBY_ZA	1 – Z accelerometer is disabled. 0 – Z accelerometer is on.
[2:0]	-	Reserved.

9.20 REGISTERS 114 AND 115 – FIFO COUNT REGISTERS

Register Name: FIFO_COUNTH

Register Type: READ Only

Register Address: 114 (Decimal); 72 (Hex)

BIT	NAME	FUNCTION
[7:5]	-	Reserved.
[4:0]	FIFO_COUNT[12:8]	High Bits; count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

Register Name: FIFO_COUNTL

Register Type: READ Only

Register Address: 115 (Decimal); 73 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_COUNT[7:0]	Low Bits; count indicates the number of written bytes in the FIFO. **Note**: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

9.21 REGISTER 116 – FIFO READ WRITE

Register Name: FIFO_R_W

Register Type: READ/WRITE

Register Address: 116 (Decimal); 74 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_DATA[7:0]	Read/Write command provides Read or Write operation for the FIFO.

Description:

This register is used to read and write data from the FIFO buffer.

Data are written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data are available. Normal data are precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

9.22 REGISTER 117 – WHO AM I

Register Name: WHO_AM_I

Register Type: READ only

Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	**WHOAMI**	**Register to indicate to user which device is being accessed.**

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0xB6. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the IAM-20381 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

9.23 REGISTERS 119, 120, 122, 123, 125, 126 ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H

Register Type: READ/WRITE

Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the X accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: XA_OFFSET_L

Register Type: READ/WRITE

Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the X accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	This bit is set during factory calibration and the value must be kept unchanged.

Register Name: YA_OFFSET_H

Register Type: READ/WRITE

Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the Y accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: YA_OFFSET_L

Register Type: READ/WRITE

Register Address: 123 (Decimal); 7B (Hex)

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the Y accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved. This bit is set during factory calibration and the value must be kept unchanged.

Register Name: ZA_OFFSET_H

Register Type: READ/WRITE

Register Address: 125 (Decimal); 7D (Hex)

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Bits 14 to 7 of the 15-bit of the Z accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.

Register Name: ZA_OFFSET_L

Register Type: READ/WRITE

Register Address: 126 (Decimal); 7E (Hex)

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Bits 6 to 0 of the 15-bit of the Z accelerometer offset cancellation (2's complement). ±16g Offset cancellation in all Full-Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved. This bit is set during factory calibration and the value must be kept unchanged.

10 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

Figure 13 below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

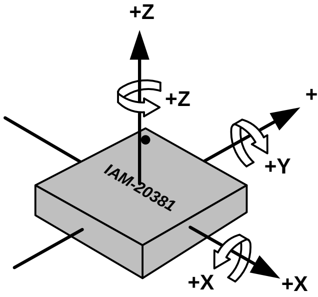
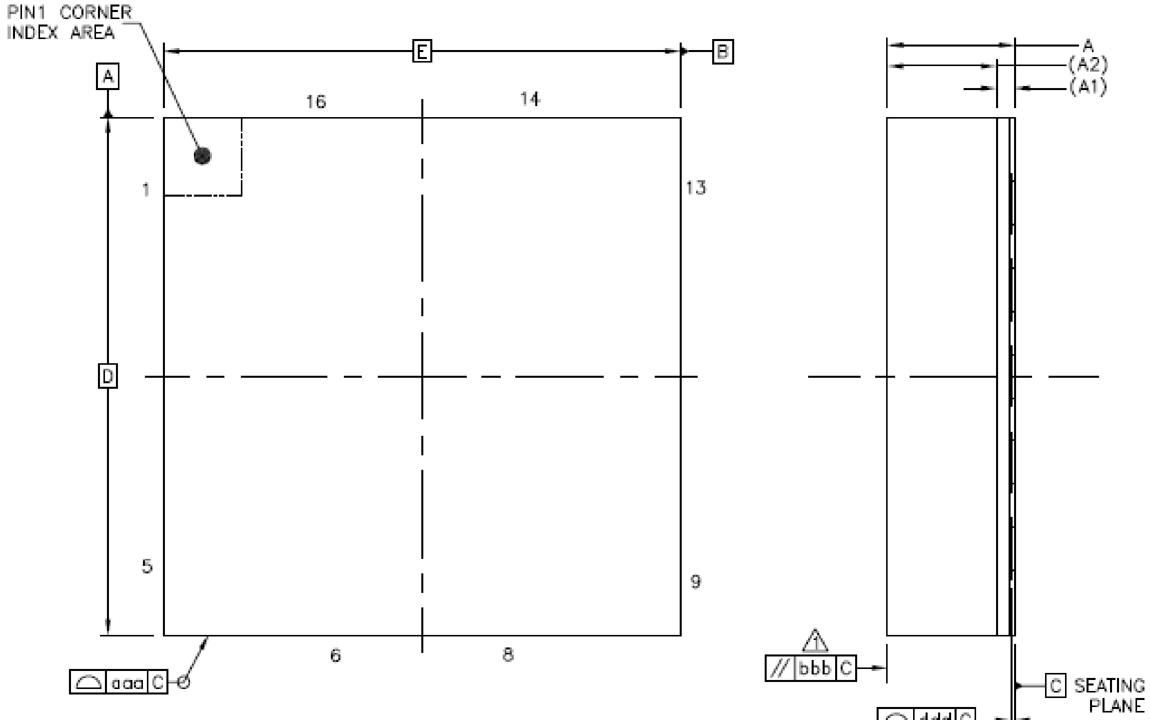


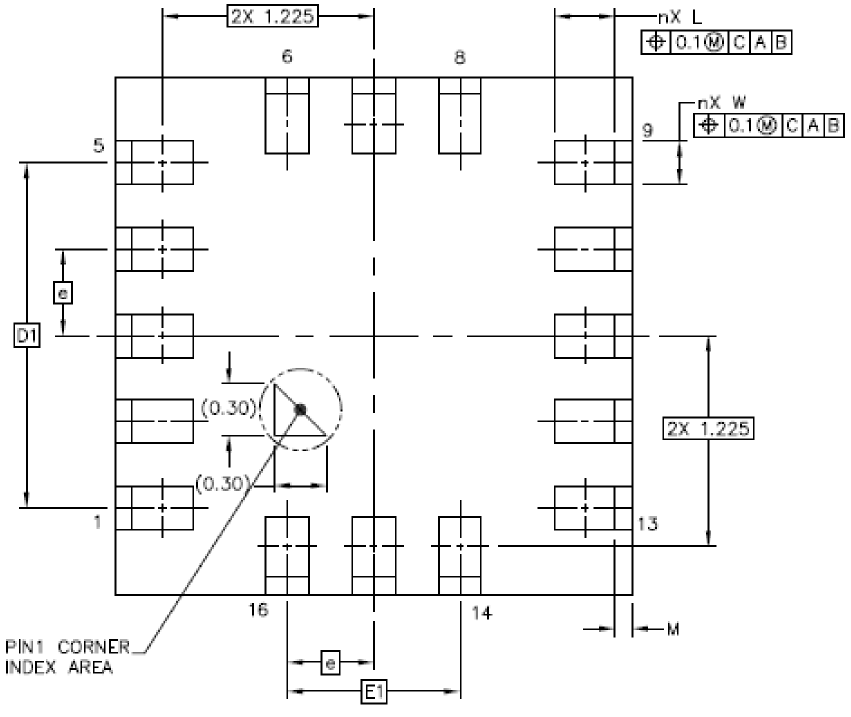
Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

10.2 PACKAGE DIMENSIONS

16 Lead LGA 3x3x0.75 mm^3 NiAu pad finish



(TOP VIEW)



(BOTTOM VIEW)

Figure 14. Package Dimensions

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	**A**	0.7	0.75	0.8
Substrate Thickness	**A1**		0.105	REF
Mold Thickness	**A2**		0.63	REF
Body Size	**D**	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	**W**	0.2	0.25	0.3
Lead Length	**L**	0.3	0.35	0.4
Lead Pitch	**e**		0.5	BSC
Lead Count	**n**		16	
Edge Ball Center to Center	**D1**		2	BSC
	E1		1	BSC
Body Center to Contact Ball	**SD**		---	BSC
	SE		---	BSC
Ball Width	**b**	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	**e1**		---	
Ball Count	**n1**		---	
Pre-Solder		---	---	---
Package Edge Tolerance	**aaa**		0.1	
Mold Flatness	**bbb**		0.2	
Coplanarity	**ddd**		0.08	
Ball Offset (Package)	**eee**		---	
Ball Offset (Ball)	**fff**		---	
Lead Edge to Package Edge	**M**	0.05	0.06	0.15

Table 18. Package Dimensions

11 PART NUMBER PACKAGE MARKING

The part number package marking for IAM-20381 devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
IAM-20381	IA2381

Table 19. Part Number Package Marking

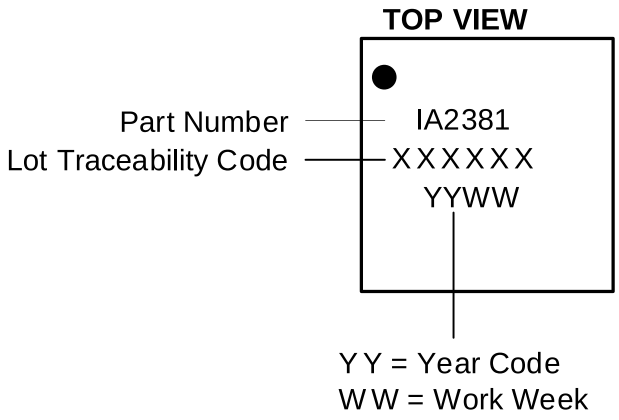


Figure 15. Part Number Package Marking

Samples with Part Number Package Marking “IA2381 E” are engineering samples and may have deviations in respect to the specifications and functions reported in the datasheet. Engineering samples are not production-intent parts.

12 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
    - Assembly Guidelines and Recommendations
    - PCB Design Guidelines and Recommendations
    - MEMS Handling Instructions
    - ESD Considerations
    - Reflow Specification
    - Storage Specifications
    - Package Marking Specification
    - Tape & Reel Specification
    - Reel & Pizza Box Label
    - Packaging
    - Representative Shipping Carton Label
- Compliance
    - Environmental Compliance
    - DRC Compliance
    - Compliance Declaration Disclaimer

13 ERRATA

Part Number	Errata Item#	Datasheet revision with Errata	Type of Errata	Technical change	Description
IAM-20381	1	Rev. 1.1	Description of behavior	No	Power mode at start-up
IAM-20381	2	Rev. 1.1	Description of behavior	No	WOM ODR configuration bits

13.1 ERRATA ITEM #1: POWER MODE AT START-UP

Background	DS-000206 revision 1.1 reported that device will come up in sleep mode upon power-up. DS-000206 revision 1.1 reported PWR_MGMT_1 default value is 0x40.
Correction in Datasheet Rev. 1.2	IAM-20381 will come up in Low-Noise Mode upon power up. PWR_MGMT_1 default value is 0x01.
Affected Sections	Section 8, Section 9, Section 9.18
Impact	No impact on component functionality. The component is in Low-Noise Mode after start-up. No change in component settings is needed for normal operation.
Workaround	To select the sleep mode at power-up, the SLEEP bit must be set to '1' into PWR_MGMT_1 register when soft reset is completed.

13.2 ERRATA ITEM #2: WOM ODR CONFIGURATION BITS

Background	DS-000206 revision 1.1 instructed to use SMPLRT_DIV register to change Accelerometer ODR in Low-power mode / WoM mode.
Correction in Datasheet Rev. 1.1	ACCEL_WOM_ODR_CTRL[3:0] bits have been documented to change the Accelerometer ODR in Low-power mode / WoM mode.
Affected Sections	Section 5.1, Table 17, Section 9.6
Impact	SMPLRT_DIV does not perform any Accelerometer ODR change when ACCEL_CYCLE is set to '1' (Low power mode).
Workaround	ACCEL_WOM_ODR_CTRL[3:0] bit field must be used to change the Accelerometer ODR in WoM mode (ACCEL_CYCLE is set to '1').

14 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
03/29/2017	1.0	Initial release
01/30/2018	1.1	Added automotive in the document title, added sections “Thermal Information section” and “Sensor Initialization and Basic Configuration”
06/08/2021	1.2	Updated Page 1 Footer Disclaimer Section 3.1: clarified typical operating conditions, Full Scale and Low-Noise Mode Table 7: Updated Electrostatic Discharge (ESD) Protection, removed MM, added CDM Section 4.12: Updated items that can generate interrupt (section incorrectly reported that the clock generator interrupt and the accelerometer can generate interrupts) Table 9: Updated wording on table’s Note Section 4.17.1 Added Power up sequence description Section 4.17.2 Updated Sensor Initialization and Clock source selection, improved description Section 4.17.3 Added Digital Interface Access test Section 5.1: Improved Wake on Motion configuration description, added LP_MODE_CFG to change WoM ODR Section 8: Added LP_MODE_CFG register Section 8: Added self-test registers and Offset registers in the not 0x00 registers list Table 17: Documented ACCEL_WOM_ODR_CTRL bit field to change ODR in low-power mode Added Section 9.6: Low power mode configuration register LP_MODE_CFG Section 9.7: Added wake on motion threshold resolution Section 9.23: Improved registers function description Figure 14: Updated package dimension Image Table 18: Corrected Lead Edge to Package Edge dimension Section 11: Corrected package marking, section incorrectly reported IA238 instead od IA2381 Section 13: Added Errata

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